APPENDIX

131. A processor comprising:

a register file having a plurality of registers;

an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;

a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in bundles, each bundle including a plurality of instructions and a template field grouped together in a N-bit field, the instructions being located in instruction slots of the N-bit field, the template field specifying a mapping of the instruction slots to the execution unit types.

132. The processor of claim 131 wherein the template field further specifies instruction group boundaries within the bundle, with an instruction group comprising a set of statically contiguous instructions that are executed concurrently.

133. The processor of claim 132 wherein the instruction types include integer arithmetic logic unit, memory, floating-point, and branch instructions.

134. A processor comprising:

a register file having a plurality of registers;

an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;

a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in bundles, each bundle including a plurality of instructions and a template field grouped together in a N-bit field, the instructions being located in instruction slots of the N-bit field, the template field specifying a mapping of the instruction slots to the execution unit types, at least one encoding of the template field further specifying instruction group boundaries within a bundle, with an

instruction group comprising a set of statically contiguous instructions that are executed concurrently.

135. The processor of claim 134 wherein the instruction types include integer arithmetic logic unit, memory, floating-point, and branch instructions.

136. The processor of claim 134 wherein each bundle further includes a stop-bit that specifies an inter-bundle instruction group boundary.

137. A processor comprising:

a register file having a plurality of registers;

an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;

a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in bundles, each bundle including a plurality of instructions, a stop bit, and a template field grouped together in a N-bit field, the instructions being located in instruction slots of the N-bit field, the template field specifying a mapping of the instruction slots to the execution unit types, at least one encoding of the template field further specifying instruction group boundaries within a bundle, with an instruction group comprising a set of statically contiguous instructions that are executed concurrently, the stop bit specifying an inter-bundle instruction group boundary.

138. A processor comprising:

a register file having a plurality of registers;

an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;

a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in bundles, each bundle including a plurality of instructions and a template field grouped together in a N-bit field, the

instructions being located in instruction slots of the N-bit field, the template field specifying a mapping of the instruction slots to the execution unit types, an unused encoding of the template field being available for use in a future extension of the processor.

139. (Amended) A processor comprising:

a register file having a plurality of registers;

an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;

a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in frames, each frame including a plurality of instructions and routing data grouped together in an N-bit field, the instructions being located in instruction positions of the N-bit field, the routing data specifying a routing of the instructions in the instruction positions to the execution unit types;

wherein the routing data is not primarily determined by hardware.

140. The processor of claim 139 wherein the routing data further specifies instruction groups that are executed sequentially within the frames, with an instruction group comprising a set of statically contiguous instructions that are executed concurrently.

141. The processor of claim 140 wherein the instruction types include integer arithmetic logic unit, memory, floating-point, and branch instructions.

142. A processor comprising:

a register file having a plurality of registers;

an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;

a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in frames, each frame including a plurality of instructions and routing data grouped together in an N-bit field, the

mapping of the instruction slots to the execution unit types, an unused encoding of the template field being available for use in a future extension of the processor.

139. A processor comprising:
a register file having a plurality of registers;
an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;
a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;
and further wherein the instructions are encoded in frames, each frame including a plurality of instructions and routing data grouped together in an N-bit field, the instructions being located in instruction positions of the N-bit field, the routing data specifying a routing of the instructions in the instruction positions to the execution unit types.

140. The processor of claim 139 wherein the routing data further specifies instruction groups that are executed sequentially within the frames, with an instruction group comprising a set of statically contiguous instructions that are executed concurrently.

141. The processor of claim 140 wherein the instruction types include integer arithmetic logic unit, memory, floating-point, and branch instructions.

142. A processor comprising:
a register file having a plurality of registers;
an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;
a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;
and further wherein the instructions are encoded in frames, each frame including a plurality of instructions and routing data grouped together in an N-bit field, the instructions being located in placed positions of the N-bit field, the routing data specifying a mapping of the instruction in the placed positions to the execution unit types, at least one encoding of the routing data further specifying instruction group boundaries within a frame, with an instruction group comprising a set of statically contiguous instructions that are executed concurrently.

143. The processor of claim 142 wherein the instruction types include integer arithmetic logic unit, memory, floating-point, and branch instructions.

144. The processor of claim 142 wherein the routing data specifies inter-frame instruction groups that are executed sequentially.

145. A processor comprising:
a register file having a plurality of registers;
an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;
a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in frames, each frame including a plurality of instructions, and routing data grouped together in an N-bit field, the instructions being located in instruction slots of the N-bit field, the routing data specifying a mapping of the instruction slots to the execution unit types, at least one encoding of the routing data field further specifying instruction group boundaries within a frame, with an instruction group comprising a set of statically contiguous instructions that are executed concurrently, the routing data specifying instruction groups within the frame that are executed sequentially.

146. A processor comprising:

a register file having a plurality of registers;

an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;

a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in frames, each frame including a plurality of instructions and routing data grouped together in an N-bit field, the instructions being located in set positions of the N-bit field, the routing data specifying a mapping of the instruction in the set positions to the execution unit types, an unused encoding of the routing data being available for use for later expansion with additional pipeline processor types.

instructions being located in placed positions of the N-bit field, the routing data specifying a mapping of the instruction in the placed positions to the execution unit types, at least one encoding of the routing data further specifying instruction group boundaries within a frame, with an instruction group comprising a set of statically contiguous instructions that are executed concurrently.

143. The processor of claim 142 wherein the instruction types include integer arithmetic logic unit, memory, floating-point, and branch instructions.

144. The processor of claim 142 wherein the routing data specifies inter-frame instruction groups that are executed sequentially.

145. A processor comprising:

a register file having a plurality of registers;

an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;

a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in frames, each frame including a plurality of instructions, and routing data grouped together in an N-bit field, the instructions being located in instruction slots of the N-bit field, the routing data specifying a mapping of the instruction slots to the execution unit types, at least one encoding of the routing data field further specifying instruction group boundaries within a frame, with an instruction group comprising a set of statically contiguous instructions that are executed concurrently, the routing data specifying instruction groups within the frame that are executed sequentially.

146. A processor comprising:

a register file having a plurality of registers;

an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;

a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;

and further wherein the instructions are encoded in frames, each frame including a plurality of instructions and routing data grouped together in an N-bit field, the instructions being located in set positions of the N-bit field, the routing data specifying a mapping of the instruction in the set positions to the execution unit types, an unused encoding of the routing data being available for use for later expansion with additional pipeline processor types.